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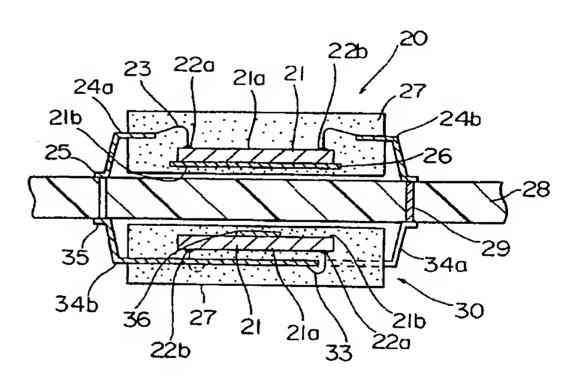
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- 64 Method of manufacturing inversion type ICs and IC module using same.
- A method of manufacturing inversion type ICs includes connecting a first electrode pad group 22a of a semiconductor chip 21 to an opposite lead group 34b via wires 33; connecting a second electrode pad group 22b to a further lead group 34a via wires; sealing the semiconductor chip, the first and second lead groups and the wires by a resin so that the outer lead portions of the leads are exposed; and bending the outer lead portions of the leads towards the bottom surface of the semiconductor chip. An IC module includes: a mounting substrate 28; a standard type IC 20; an inversion type IC 30 which is mounted on the bottom surface of the mounting substrate so that the leads having the same function as those of the standard type IC come to the same point with the mounting substrate in between, first and second electrode pad groups 22a, 22b formed on the surface of the semiconductor chip being connected via wires to second and first lead groups 34b, 34a, respectively, and the outer lead portions of the leads being bent towards the bottom surface of the semiconductor chip; and a plurality of connecting members, provided on the mounting substrate, for electrically connecting the leads of the standard type IC and the leads of the inversion type IC having the same function as those of the standard type IC.

FIG.I



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BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION:

The present invention relates to a method of manufacturing inversion type ICs for high-density mounting and to an IC module in which inversion ICs are mounted.

DESCRIPTION OF THE RELATED ART:

The construction of a conventional resin seal type IC 8 is shown in Fig. 18. A semiconductor chip 1 is mounted on a die pad 11. An electrode pad 2 formed on a surface 1a of the semiconductor chip 1 is electrically connected to an inner lead portion of a corresponding lead 4 by a wire 3. The semiconductor chip 1, the wire 3, the inner lead portion of the lead 4 and the die pad 11 are sealed by a main body of a package 5 made of a resin so that an outer lead portion 6 of the lead 4 is exposed. The outer lead portion 6 of each lead 4 is usually bent toward the bottom surface 1b of the semiconductor chip 1 in order to mount the IC.

When a plurality of ICs constructed as described above are mounted on a single mounting substrate and, for example, when a large-capacity storage device is formed, leads of the same pin numbers of a plurality of leads having the same functions must be connected to each other. When, for example, a plurality of ICs are mounted on both sides of a mounting substrate, since the pin arrangement of ICs mounted on the top surface of the mounting substrate does not match the IC pin arrangement mounted on the bottom surface, leads having the same functions do not match each other. Also, when a plurality of ICs are mounted on a single surface of a mounting substrate, leads having the same functions do not meet each other in adjacent ICs. As a consequence, there is a problem in that, since leads having the same functions are connected to each other, wiring on a mounting substrate becomes complex.

A method shown in Fig. 19 for solving such a problem is disclosed in Japanese Utility Model Laid-Open No. 62-16865. In this method, ICs, such as ICs 9, are formed, in which the pin connection is inverted by bending the outer lead portion 6 toward the top surface 1a of the semiconductor chip 1, in contrast with standard ICs, such as ICs 8, in which the outer lead portion 6 is bent toward the bottom surface 1b of the semiconductor chip 1. A standard IC 8 is mounted on a top surface 7a of a mounting substrate 7, and an inversion IC 9 is mounted on a bottom surface 7b thereof. With this construction, leads corresponding to each other can be connected easily by merely providing a through hole 10 on the mounting substrate 7 because the leads of the same pin numbers of both ICs 8 and 9 come to the same point with the mounting

substrate 7 inbetween.

However, if an ultra-thin package, such as a TSOP (Thin Small Outline Package) having a thickness of approximately 1 mm, is mounted as shown in Fig. 19, the following problem occurs. Since the thickness is thin, the outer lead portion 6 exposed to the outside from the main body 5 of the package is short. If heat stress, such as heat cycle, is applied thereto, the solder connection portion between the outer lead portion 6 and the mounting substrate 7 is destroyed by a short cycle. For this reason, although it may seem that, to absorb heat stress, for example, a lead guide surface of the IC 8 should be made higher and the length L1 from the lead guide surface to the mounting substrate 7 made longer, in the inversion type ICs 9, on the contrary, the length L2 from the lead guide surface to the mounting substrate 7 becomes short, and the performance deteriorates.

In addition, there is another problem in that, productivity is lowered since the shapes of the bent leads are different for ICs 8 and 9 and two types of dies for bending operations are required to manufacture standard and inversion type ICs.

SUMMARY OF THE INVENTION

The present invention has been achieved to solve the above-mentioned problems of the prior art.

An object of the present invention is to provide a method of manufacturing highly reliable inversion ICs which can be mounted in high densities with simple wirings.

Another object of the present invention is to provide highly reliable IC modules which uses such inversion ICs.

To these ends, according to the present invention, there is provided a method of manufacturing inversion type ICs by using semiconductor chips which are the same as for standard ICs in which first and second electrode pad groups are connected via wires to first and second lead groups, respectively, all of which are formed on a surface of a semiconductor chip, and the outer lead portions of the leads are bent toward the bottom surface of the semiconductor chip, the pin connection thereof being inverted, the method including the steps of: connecting a first electrode pad group of a semiconductor chip to a second lead group via wires; connecting a second electrode pad group of the semiconductor chip to a first lead group via wires; sealing the semiconductor chip, the first and second lead groups and the wires by a resin so that the outer lead portions of the leads are exposed; and bending the outer lead portions of the leads toward the bottom surface of the semiconductor chip.

According to one aspect, the present invention which achieves these objectives relates to an IC module including a mounting substrate; a standard type IC, mounted on a surface of the mounting substrate,

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in which first and second electrode pad groups formed on the surface of the semiconductor chip are connected via wires to first and second lead groups, respectively, and the outer lead portions of the leads are bent toward the bottom surface of the semiconductor chip; an inversion type IC which is mounted on the bottom surface of the mounting substrate so that the leads having the same function as those of the standard type IC come to the same point with the mounting substrate inbetween, first and second electrode pad groups formed on the surface of the semiconductor chip being connected via wires to second and first lead groups, respectively, and the outer lead portions of the leads being bent toward the bottom surface of the semiconductor chip; and a plurality of connecting members, provided on the mounting substrate, for electrically connecting the leads of the standard type IC and the leads of the inversion type IC having the same function as those of the standard type IC.

According to another aspect, the present invention which achieves these objectives relates to an IC module including: a mounting substrate; a standard type IC, mounted on a surface of the mounting substrate, in which first and second electrode pad groups formed on the surface of the semiconductor chip are connected via wires to first and second lead groups, respectively, and the outer lead portions of the leads are bent toward the bottom surface of the semiconductor chip; and an inversion type IC which is mounted on the surface of the mounting substrate so that the leads thereof and the leads of the standard type IC having the same function as those of the inversion type IC are adjacent to each other and electrically connected to each other, first and second electrode pad groups formed on the surface of the semiconductor chip being connected via wires to second and first lead groups, respectively, and the outer lead portions of the leads being bent toward the bottom surface of the semiconductor chip.

According to the method of manufacturing inversion ICs of the present invention, first and second electrode pad groups formed on a surface of a semiconductor chip are connected via wires to second and first lead groups, respectively, in a manner opposite to that in the standard type IC, and the outer lead portions of each of the leads are bent toward the bottom surface of the semiconductor chip in the same manner as in the standard type IC.

In the IC module, a standard type IC is mounted on a surface of a mounting substrate, whereas an inversion type IC manufactured by the method described in claim 1 is mounted on the bottom surface of the mounting substrate. The leads of the standard type IC and the inversion type IC, having the same functions, are arranged so that they come to the same point with the mounting substrate inbetween, and are electrically connected to each other by connection mem-

bers.

In an IC module according to another aspect of the present invention, the standard type IC and the inversion type IC manufactured by the method described in claim 1 are both mounted on the surface of the mounting substrate, and the leads of the standard type IC and the inversion type IC, having the same functions, are arranged adjacent to each other and are electrically connected to each other.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view illustrating an IC module according to a first embodiment of the present invention;

Fig. 2 is a perspective plan view illustrating a standard type IC used in the first embodiment of the present invention;

Fig. 3 is a cross-sectional view taken along the line A-A of Fig. 2;

Fig. 4 is a perspective plan view illustrating an inversion type IC used in the first embodiment;

Fig. 5 is a cross-sectional view taken along the line B-B of Fig. 4;

Fig. 6 is a cross-sectional view illustrating an IC module according to a second embodiment of the present invention;

Fig. 7 is a perspective plan view illustrating a standard type IC used in the second embodiment of the present invention;

Fig. 8 is a cross-sectional view taken along the line C-C of Fig. 7;

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Fig. 9 is a perspective plan view illustrating an inversion type IC used in the second embodiment; Fig. 10 is a cross-sectional view taken along the line D-D of Fig. 9;

Fig. 11 is a perspective plan view illustrating a standard type IC used in the third embodiment of the present invention;

Fig. 12 is a cross-sectional view taken along the line E-E of Fig. 11;

Fig. 13 is a perspective plan view illustrating an inversion type IC used in the third embodiment of the present invention;

Fig. 14 is a cross-sectional view taken along the line F-F of Fig. 13;

Fig. 15 is a perspective plan view illustrating an inversion type IC used in a modification of the first embodiment of the present invention;

Fig. 16 is a cross-sectional view taken along the line G-G of Fig. 15;

Fig. 17 is a cross-sectional view illustrating an IC module according to a fourth embodiment of the present invention;

Fig. 18 is a cross-sectional view illustrating a conventional IC; and

Fig. 19 is a cross-sectional view illustrating a conventional IC module.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be explained below with reference to the accompanying drawings.

In Fig. 1, a standard type IC 20 is mounted on the top surface of a mounting substrate 28, and an inversion type IC 30 is mounted on the bottom surface thereof. The standard type IC 20 has a die pad 26, as shown in Figs. 2 and 3. A semiconductor chip 21 is mounted on the die pad 26. First and second electrode pad groups 22a and 22b are formed on a surface 21a of the semiconductor chip 21 along both sides of the length of the semiconductor chip 21. A first lead group 24a formed of leads 1 through 13 and a second lead group 24b formed of leads 14 through 26 are arrayed in the vicinity of the long sides of the semiconductor chip 21. Each of the electrode pads of the first electrode pad group 22a of the semiconductor chip 21 is electrically connected via wires 23 to a corresponding inner lead portion of the leads of the first lead group 24a. Likewise, each of the electrode pads of the second electrode pad group 22b is electrically connected via the wires 23 to a corresponding inner lead portions of the leads of the second lead group 24b. The semiconductor chip 21, the wires 23, the inner lead portion of each of the leads, and the die pad 26 are sealed by a main body of a package 27 made of a resin so that the outer lead portions 25 of the leads of the first and second lead groups 24a and 24b are exposed. The outer lead portion 25 of each of the leads is bent toward the bottom surface 21b of the semiconductor chip 21.

On the other hand, the inversion type IC 30 has a die pad 36, as shown in Figs. 4 and 5. The semiconductor chip 21 similar to that used in the standard type IC 20 is mounted on the die pad 36. A first lead group 34a formed of leads 1 through 13 and a second lead group 34b formed of leads 14 through 26 are alternately arrayed above the semiconductor chip 21. Contrary to the standard type IC 20, each of the electrode pads of the first electrode pad group 22a of the semiconductor chip 21 is electrically connected via wires 33 to the corresponding inner lead portion of the leads of the second lead group 34b, while each of the electrode pads of the second electrode pad group 22b of the semiconductor chip 21 is electrically connected via wires 33 to the corresponding inner lead portion of the leads of the first lead group 34a. The semiconductor chip 21, the wires 33, the inner lead portion of each of the leads, and the die pad 36 are sealed by the package's main body 27 made of a resin so that the outer lead portions 35 of the leads of the first and second lead groups 34a and 34b are exposed. The outer lead portions 35 of the leads are bent toward the bottom surface 21b of the semiconductor chip 21 in the same manner as in the standard

type IC 20.

4M dynamic RAMs are shown as examples for the ICs 20 and 30. In Figs. 2 and 4, circled numerals near respective leads indicate the lead numbers of the respective leads. Letters written near respective electrode pads of the semiconductor chip 21 indicate the functions of the respective electrode pads. For example, D indicates data input; Q indicates data output; \overline{W} indicates write control input; A_0 to A_{10} indicate address input; V_{cc} indicates a power supply of 5V; and V_{ss} indicates a reference voltage of 0V.

As described above, a group of leads to which the first and second electrode pad groups 22a and 22b are connected are inverted for the standard type IC 20 and the inversion type IC 30. That is, in the standard type IC 20, the first and second electrode pad groups 22a and 22b are connected to the first lead group 24a and the second lead group 24b, respectively. In the inversion type IC 30, the first and second electrode pad groups 22a and 22b are connected to the second lead group 34b and the first lead group 34a, respectively. For this reason, for example, the electrode pad for data input is connected to the first lead of the standard type IC 20, and the electrode pad for 0V reference voltage is connected to the twentysixth lead. In contrast, the electrode pad for 0V reference voltage is connected to the first lead of the inversion type IC 30, and the electrode pad for data input is connected to the twenty-sixth lead.

Therefore, if these ICs 20 and 30 are arranged on both sides of the mounting substrate 28 as shown in Fig. 1, the leads of both ICs 20 and 30, having the same functions, come to the same point with the mounting substrate 28 inbetween. The corresponding outer lead portions 25 and 35 of these leads are electrically connected to each other via through holes 29, serving as connecting members, provided in the mounting substrate 28.

The aforesaid inversion type IC 30 can be manufactured as set forth below. First, the semiconductor chip 21 is mounted on the die pad 36. Each of the electrode pads of the first electrode pad group 22a is connected via the wires 33 to the corresponding leads of the second lead group 34b, while each of the electrode pads of the second electrode pad group 22b is connected via the wires 33 to the corresponding leads of the first lead group 34a. Next, the semiconductor chip 21, the wires 33, the inner lead portions of the respective leads, and the die pad 36 are sealed by the main body of the package 27 so that the outer lead portions 35 of the leads are exposed. Thereafter, the outer lead portions 35 of the leads are bent toward the bottom surface 21b of the semiconductor chip 21 in the same manner as in the standard type IC 20.

As shown in Fig. 1, since the leads of the ICs 20 and 30 are guided to the outside from a position deviated from the central portion of the package's main

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body 27 toward a position higher than and facing the surface 21a of the semiconductor chip 21, and bent toward the bottom surface 21b of the semiconductor chip 21, the length of the leads exposed in the outside of the package's main body 27 can be taken long. As a result, reliability against heat stress after mounting is improved.

In addition, since the outer leads 35 of the leads of the inversion type IC 30 are bent toward the bottom surface 21b of the semiconductor chip 21 in the same manner as the outer leads 25 of the standard type IC 20, a die for a bending operation can be used which is common to the standard type IC 20 and the inversion type IC 30. Thus, workability and productivity are improved.

Fig. 6 shows an IC module according to the second embodiment of the present invention. A standard type IC 40 is mounted on the top surface of the mounting substrate 28, and an inversion type IC 50 is mounted on the bottom surface thereof. The standard type IC 40 is shown in Figs. 7 and 8, and the inversion type IC 50 in Figs. 9 and 10. The ICs 40 and 50 each have a semiconductor chip 41, first and second lead groups 44a and 44b, a die pad 46 and a main body of a package 47. First and second electrode pad groups 42a and 42b are formed alternately in a line traversing the longitudinal center of a surface 41a of the semiconductor chip 41. The inner lead portions of the first and second lead groups 44a and 44b are arrayed on both sides of the pad groups 42a and 42b, respectively.

As shown in Fig. 7, in the standard type IC 40, each of the electrode pads of the pad group 42a of the semiconductor chip 41 is electrically connected via corresponding wires 43 to the corresponding inner lead portions of the leads of the first lead group 44a. Each of the electrode pads of the second electrode pad group 42b is electrically connected via corresponding wires 43 to the corresponding inner lead portions of the leads of the second lead group 44b. In contrast, in the inversion type IC 50, as shown in Fig. 9, each of the electrode pads of the first electrode pad group 42a of the semiconductor chip 41 is electrically connected via corresponding wires 53 to the corresponding inner lead portions of the leads of the second lead group 44b. Each of the electrode pads of the second electrode pad group 42b is electrically connected via corresponding wires 53 to the corresponding inner lead portions of the leads of the first lead group 44a. In both the ICs 40 and 50, the outer lead portions 45 of the leads are bent toward a bottom surface 41b of the semiconductor chip 41.

As described above, when a semiconductor chip having electrode pads along its center line is used, the inversion type IC 50 can be manufactured easily by merely changing the connection of wires 43 and 53.

A standard type IC 60 used in the third embodi-

ment is shown in Figs. 11 and 12. In this IC 60, leads are guided from each of the four sides of a main body of a package 67. A semiconductor chip 61 is mounted on a die pad 66. A first lead group 64a formed of leads 1 to 6, 15 and 16, and a second lead group 64b formed of leads 7 to 14 are arranged above the semiconductor chip 61. A first electrode pad group 62a and a second electrode pad group 62b are arrayed parallel to each other on a surface 61a of the semiconductor chip 61. Each of the pads of the first electrode pad group 62a are electrically connected via corresponding wires 63 to the corresponding inner lead portions of the leads of a first lead group 64a. Each of the pads of the second electrode pad group 62b is electrically connected via corresponding wires 63 to the corresponding inner lead portions of the leads of a second lead group 64b. The outer lead portions 65 of the leads are bent toward the bottom surface 61b of the semiconductor chip 61.

In contrast, in an inversion type IC 70, as shown in Figs. 13 and 14, each of the pads of the first electrode pad group 62a of the semiconductor chip 61 is electrically connected via corresponding wires 73 to the corresponding inner lead portions of the leads of a second lead group 74b. Each of the pads of the second electrode pad group 62b is electrically connected via corresponding wires 73 to the corresponding inner lead portions of the leads of the first lead group 74a. The outer lead portions 75 of the leads are bent toward the bottom surface 61b of the semiconductor chip 61 in the same manner as in the standard type IC 60.

By combining the standard type IC 60 and the inversion type IC 70, highly reliable IC modules can be manufactured with simple wirings in the same way as in the first and second embodiments.

Although in the inversion type IC 30 used in the first embodiment, as shown in Figs. 4 and 5, the first and second lead groups 34a and 34b are arranged above the surface 21a of the semiconductor chip 21, the present invention is not limited to this case. For example, as in an inversion type IC 80 shown in Figs. 15 and 16, first and second lead groups 84a and 84b may be arranged in such a manner as to transverse the bottom surface 21b of the semiconductor chip 21. In this case, since a dedicated die pad for supporting the bottom surface 21b of the semiconductor chip 21 cannot be provided, an insulating film 88 is bonded to the bottom surface 21b, and the semiconductor chip 21 is mounted on the first and second lead groups 84a and 84b with the insulating film 88 placed therebetween. Each of the pads of the first electrode pad group 22a of the semiconductor chip 21 is connected via corresponding wires 83 to each of the leads of the second lead group 84b. Each of the pads of the second electrode pad group 22b is connected via corresponding wires 83 to each of the leads of the first lead group 84a. These elements are sealed using a resin

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by a main body of a package 87 so that the outer lead portions 85 of the leads are exposed.

Although in the first embodiment the standard type IC 20 and the inversion type IC 30 are mounted on the top and bottom surfaces of the mounting substrate 28 respectively, the present invention is not limited to this case. As shown in Fig. 17, the standard type IC 20 and the inversion type IC 30 may be mounted on the top surface of the mounting substrate 38 in such a way that they are adjacent to each other. The leads having the same functions in both ICs 20 and 30, for example, each of the leads of the second lead group 24b of the standard type IC 20 and each of the leads of the first lead group 34b of the inversion type IC 30 are adjacent to each other and electrically connected to each other. In this case, through holes need not be provided on the mounting substrate 38.

Claims

1. A method of manufacturing inversion type ICs by using semiconductor chips which are the same as for standard ICs in which first and second electrode pad groups are connected via wires to first and second lead groups, respectively, all of which are formed on a surface of a semiconductor chip, and the outer lead portions of the leads are bent toward the bottom surface of the semiconductor chip, the pin connection thereof being inverted, said method comprising the steps of:

connecting a first electrode pad group of a semiconductor chip to a second lead group via wires;

connecting a second electrode pad group of the semiconductor chip to a first lead group via wires;

sealing the semiconductor chip, the first and second lead groups and the wires by a resin so that the outer lead portions of the leads are exposed; and

bending the outer lead portions of the leads toward the bottom surface of the semiconductor chip.

- 2. A method of manufacturing inversion type ICs according to claim 1 wherein each of the leads is sealed so that the outer lead portion thereof is guided to the outside from a position deviated from the central portion of a main body of a package toward a position higher than and facing the surface of the semiconductor chip.
- 3. A method of manufacturing inversion type ICs according to claim 1 wherein the outer lead portions of the leads are bent by using a die which is the same as one used for bending the outer lead portions of the leads of a standard type IC.

4. An IC module comprising:

a mounting substrate;

a standard type IC, mounted on a surface of the mounting substrate, in which first and second electrode pad groups formed on the surface of the semiconductor chip are connected via wires to first and second lead groups, respectively, and the outer lead portions of the leads are bent toward the bottom surface of the semiconductor chip;

an inversion type IC which is mounted on the bottom surface of said mounting substrate so that the leads having the same function as those of the standard type IC come to the same point with the mounting substrate inbetween, first and second electrode pad groups formed on the surface of the semiconductor chip being connected via wires to second and first lead groups, respectively, and the outer lead portions of the leads being bent toward the bottom surface of the semiconductor chip; and

a plurality of connecting members, provided on said mounting substrate, for electrically connecting the leads of the standard type IC and the leads of the inversion type IC having the same function as those of the standard type IC.

- 5. An IC module according to claim 4 wherein the standard type IC and the inversion type IC each have a main body of a package for sealing the semiconductor chip, the first and second lead groups and the wires so that the outer lead portions of the leads are exposed, and each of the leads is guided to the outside from a position deviated from the central portion of the main body of the package toward a position higher than and facing the surface of the semiconductor chip.
- 6. An IC module according to claim 5 wherein the main body of the package is formed in a substantially rectangular shape, and each of the leads is guided to the outside from the facing sides of the main body of the package.
- 7. An IC module according to claim 5 wherein the main body of the package is formed in a substantially rectangular shape, and each of the leads is guided to the outside from the four sides of the main body of the package.
 - 8. An IC module according to claim 4 wherein the semiconductor chip is formed in a substantially rectangular shape, and the first and second electrode pad groups each are arrayed near the facing sides of and on the surface of the semiconductor chip.
 - 9. An IC module according to claim 8 wherein the

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first and second lead groups are arrayed in the inversion type IC in such a way that they transverse the bottom surface of the semiconductor chip.

- 10. An IC module according to claim 4 wherein the semiconductor chip is formed in a substantially rectangular shape, and the first and second electrode pad groups each are arrayed alternately in a line on the surface of the semiconductor chip along its longitudinal center line.
- 11. An IC module according to claim 4 wherein the semiconductor chip is formed in a substantially rectangular shape, and the first and second electrode pad groups each are arrayed parallel to each other on the surface of the semiconductor chip near its longitudinal center line.
- 12. An IC module comprising:

a mounting substrate;

a standard type IC, mounted on a surface of the mounting substrate, in which first and second electrode pad groups formed on the surface of the semiconductor chip are connected via wires to first and second lead groups, respectively, and the outer lead portions of the leads are bent toward the bottom surface of the semiconductor chip; and

an inversion type IC which is mounted on the surface of said mounting substrate so that the leads thereof and the leads of the standard type IC having the same function as those of the inversion type IC are adjacent to each other and electrically connected to each other, the first and second electrode pad groups formed on the surface of the semiconductor chip being connected via wires to the second and first lead groups, respectively, and the outer lead portions of the leads being bent toward the bottom surface of the semiconductor chip.

- 13. An IC module according to claim 12 wherein the standard type IC and the inversion type IC each have a main body of a package for sealing a semiconductor chip, the first and second lead groups and the wires so that the outer lead portions of the leads are exposed, and each of the leads is guided to the outside from a position deviated from the central portion of the main body of the package to a position higher than and facing the surface of the semiconductor chip.
- 14. An IC module according to claim 13 wherein the main body of the package is formed in a substantially rectangular shape, and each of the leads is guided to the outside from the facing sides of the main body of the package.

- 15. An IC module according to claim 13 wherein the main body of the package is formed in a substantially rectangular shape, and each of the leads is guided to the outside from the four sides of the main body of the package.
- 16. An IC module according to claim 12 wherein the semiconductor chip is formed in a substantially rectangular shape, and the first and second electrode pad groups are arrayed near the facing sides of and on the surface of the semiconductor chip.
- 17. An IC module according to claim 16 wherein the first and second lead groups are arrayed in the inversion type IC in such a way that they traverse the bottom surface of the semiconductor chip.
- 18. An IC module according to claim 12 wherein the semiconductor chip is formed in a substantially rectangular shape, and the first and second electrode pad groups each are arrayed alternately in a line traversing the longitudinal center of the surface of the semiconductor chip.
- 19. An IC module according to claim 12 wherein the semiconductor chip is formed in a substantially rectangular shape, and the first and second electrode pad groups each are arrayed parallel to each other on the surface of the semiconductor chip near its longitudinal center line.
- 20. An IC module substantially as herein described with reference to figures 1 to 5, figures 6 to 10, figures 11 to 14, figures 15 and 16, or figure 17 of the accompanying drawings.

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FIG.I

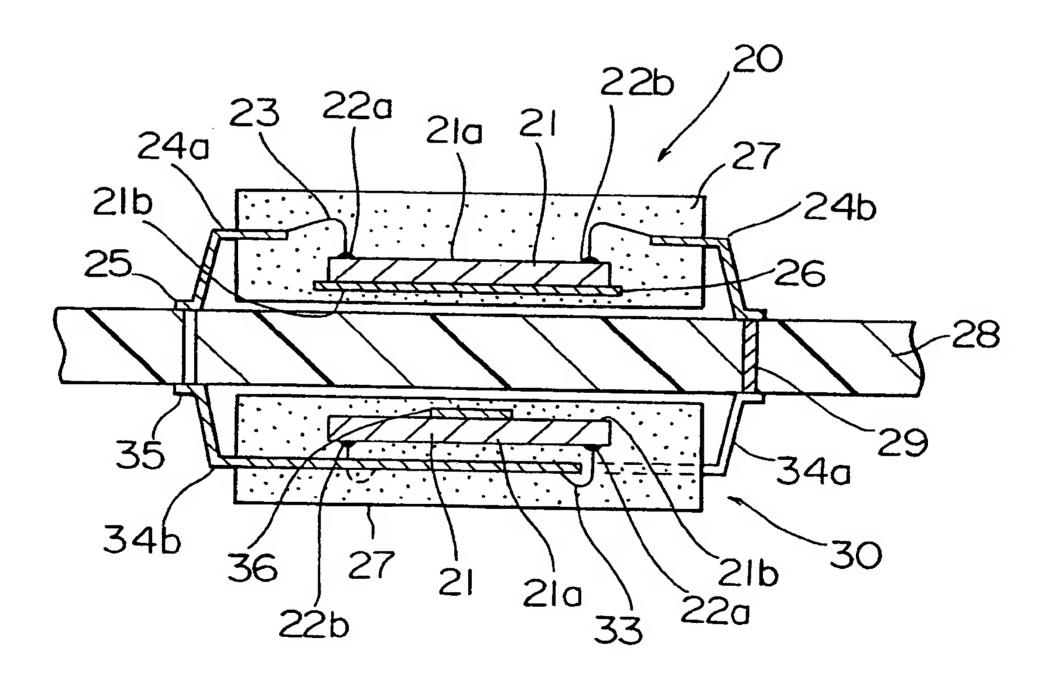


FIG.2

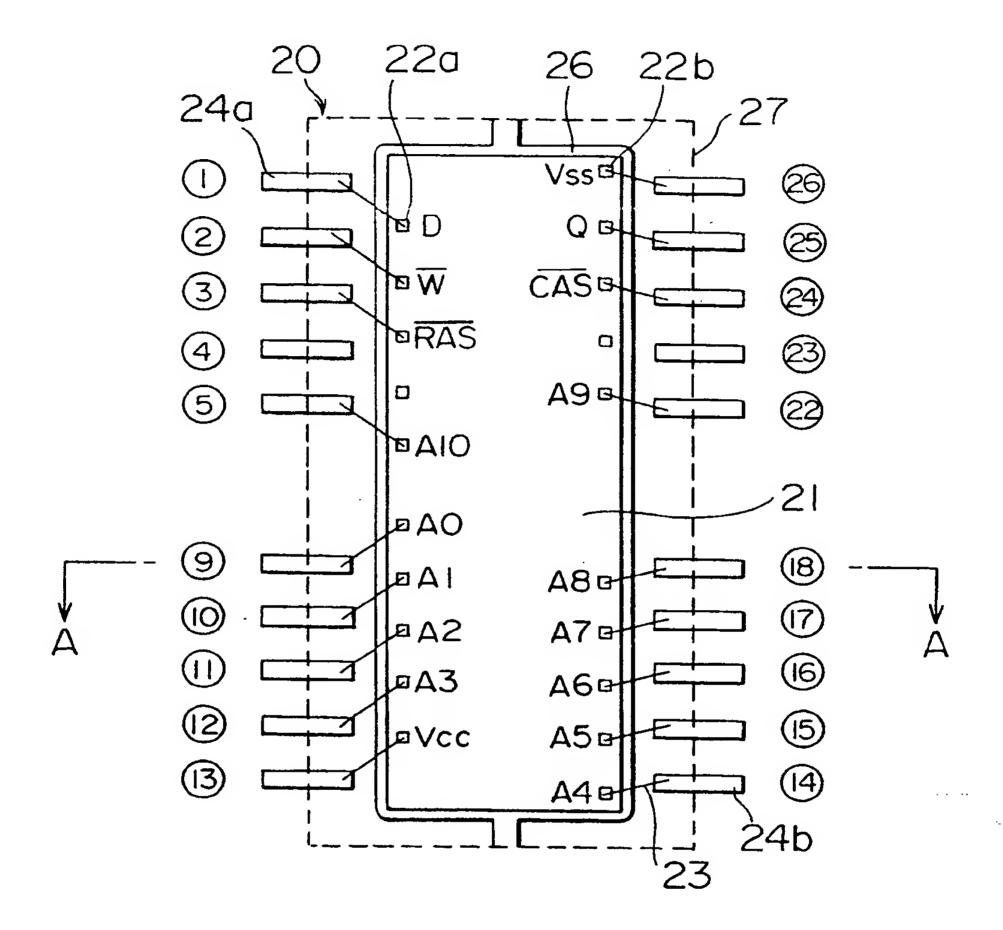


FIG.3

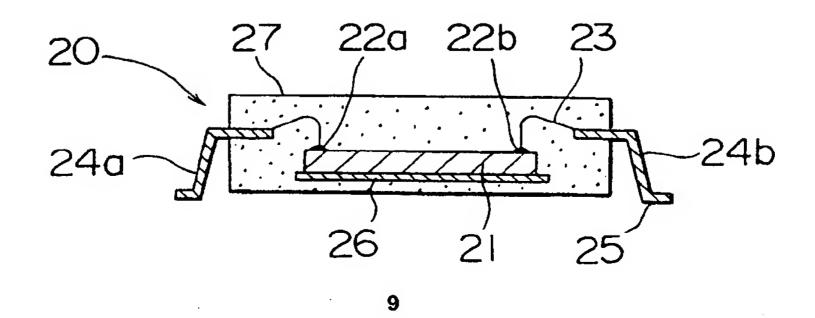


FIG. 4

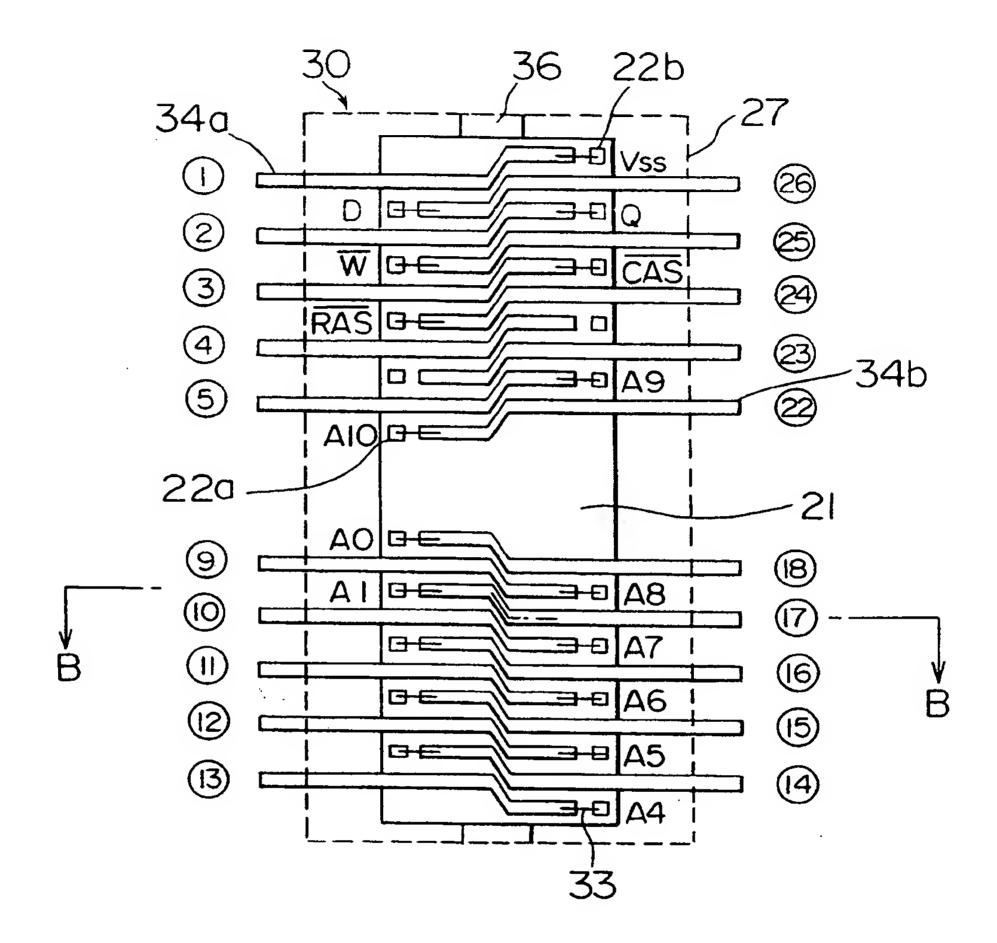


FIG.5

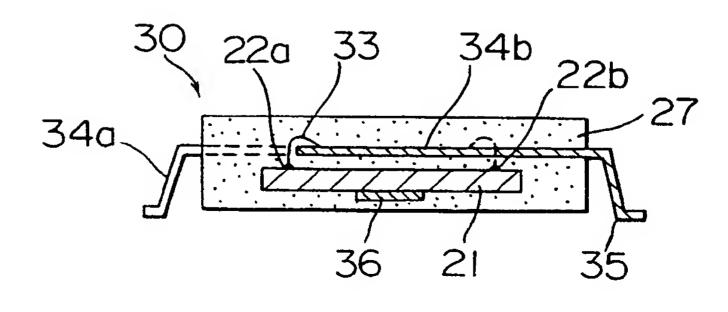


FIG.6

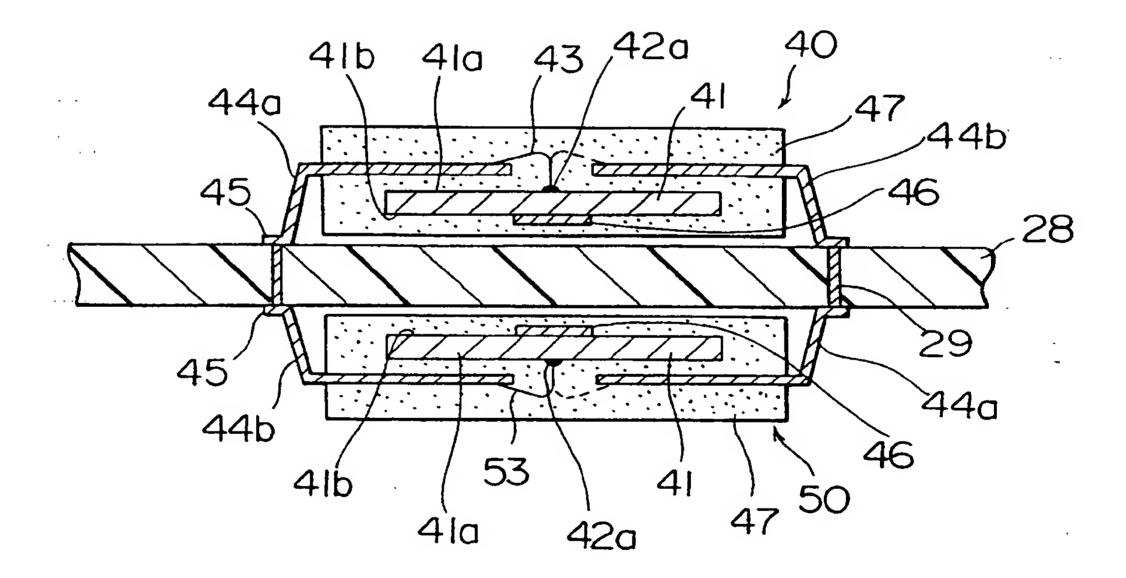
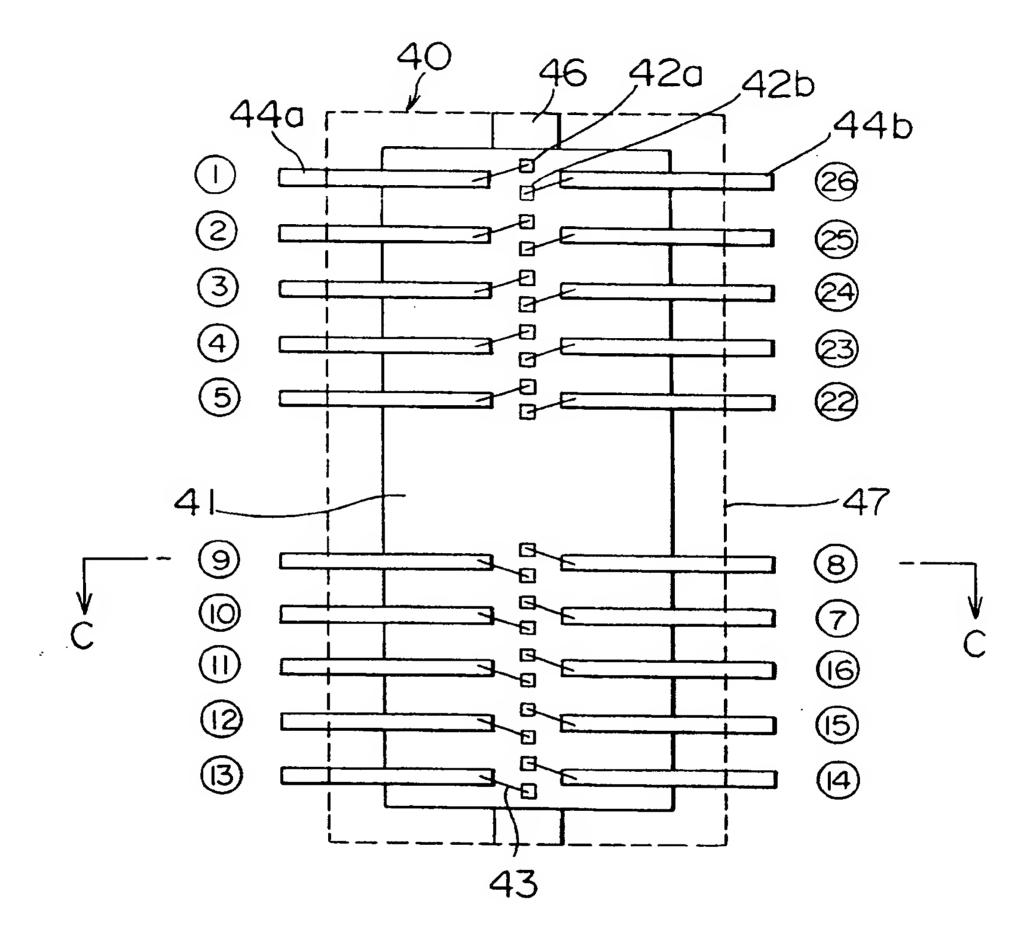


FIG.7



F 1G.8

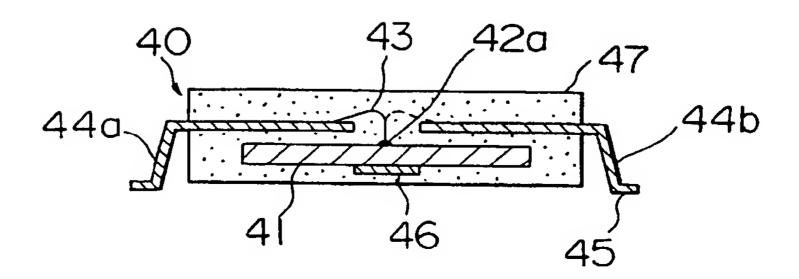
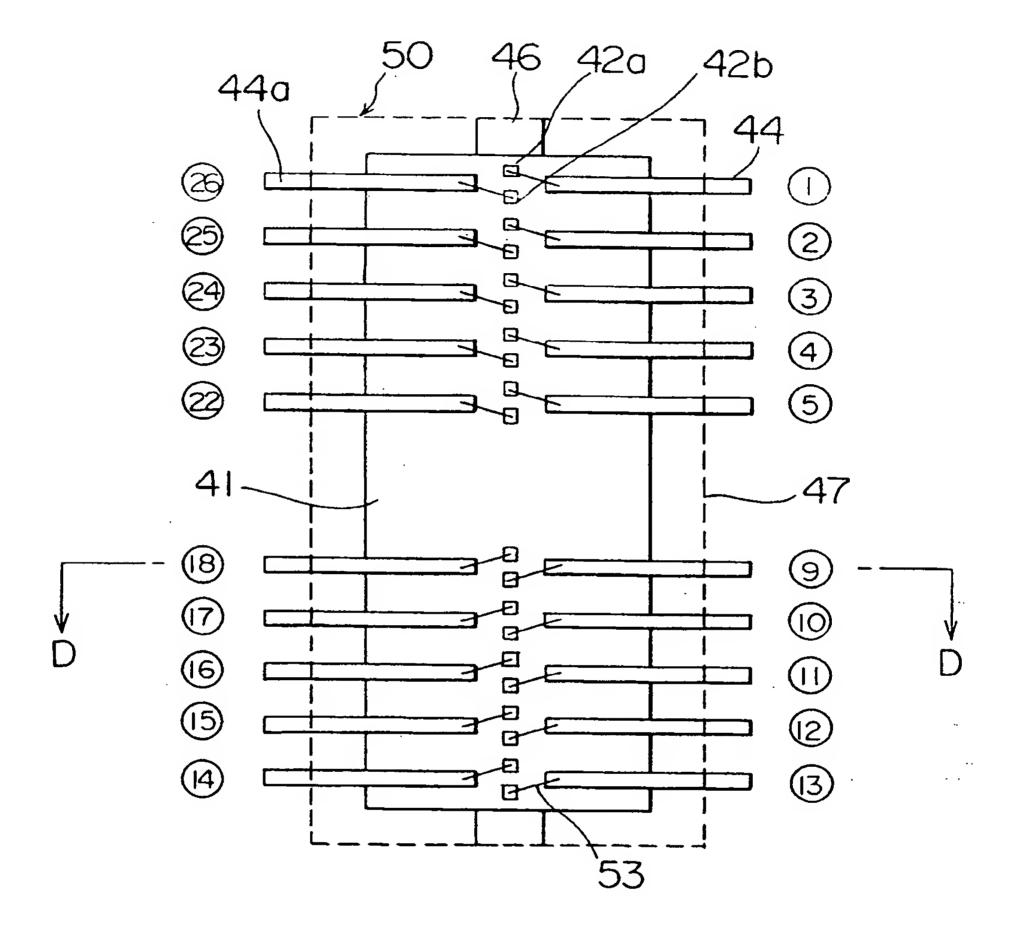


FIG.9



F 1G .10

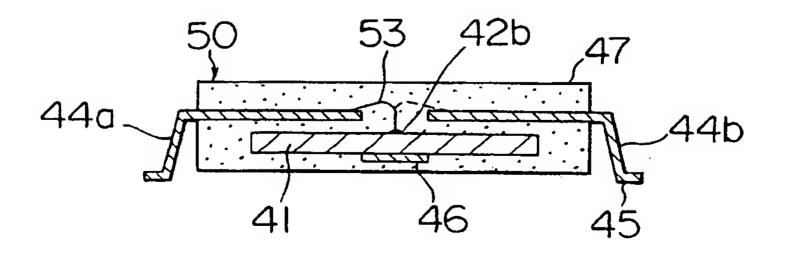


FIG.II

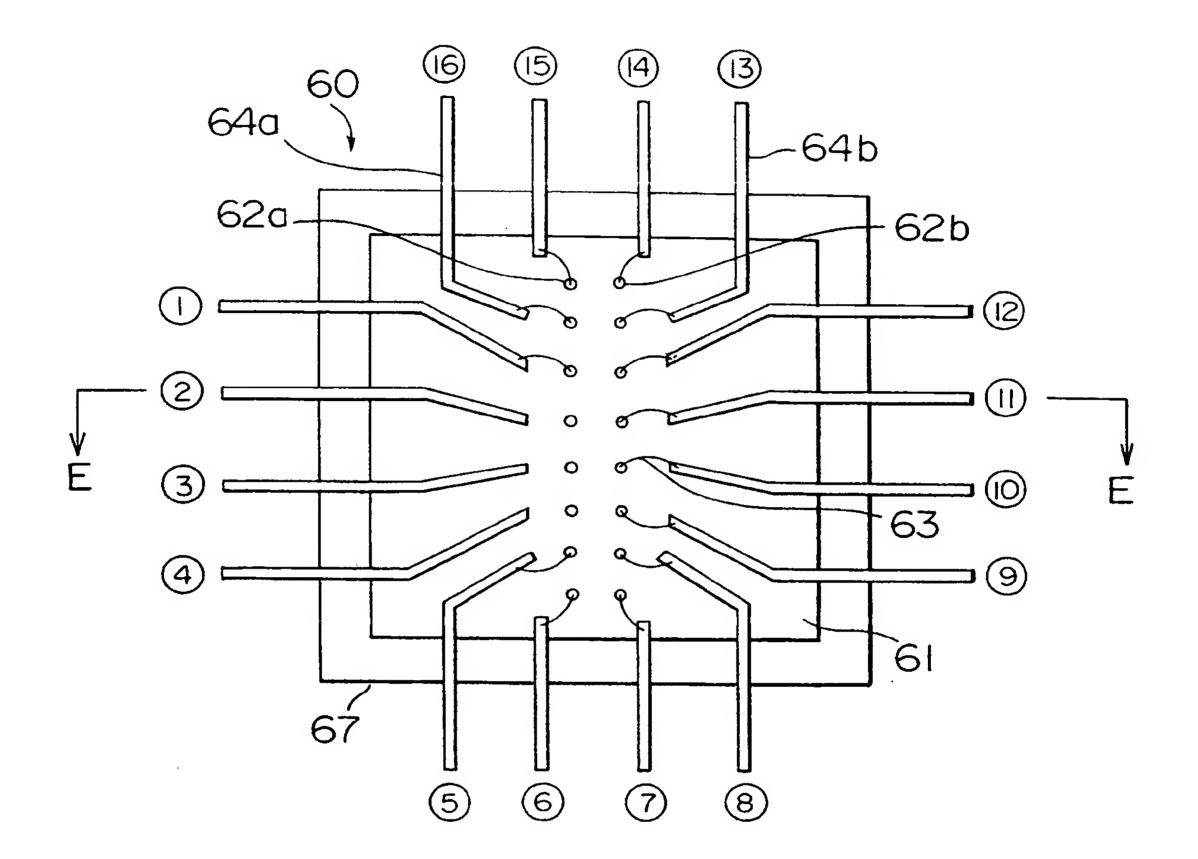
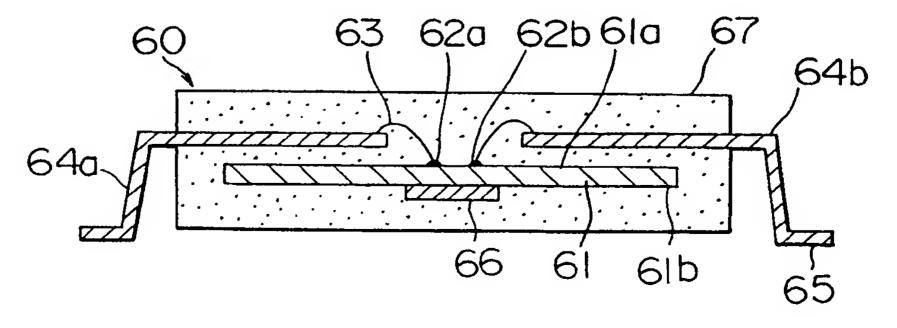


FIG.12



F IG . 13

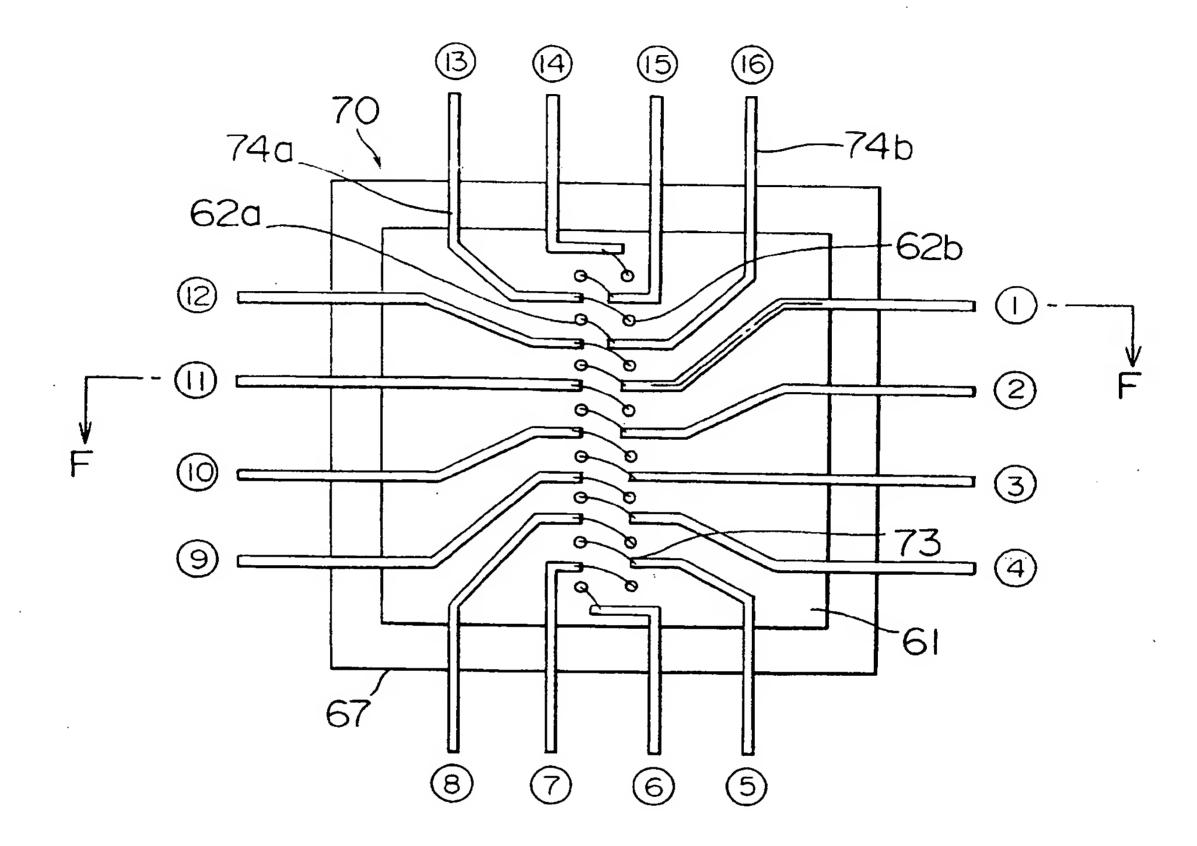


FIG. 14

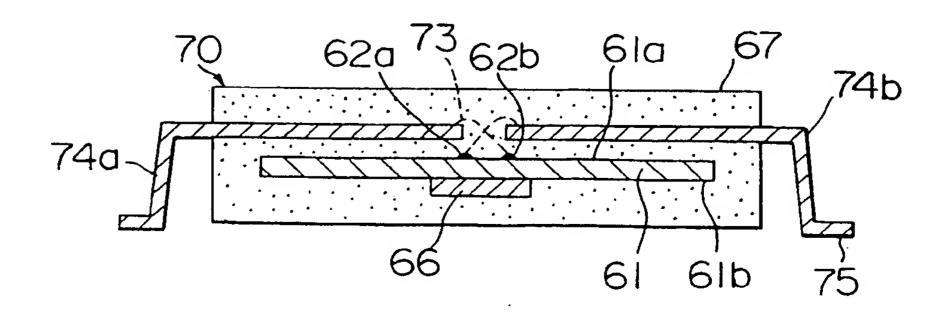
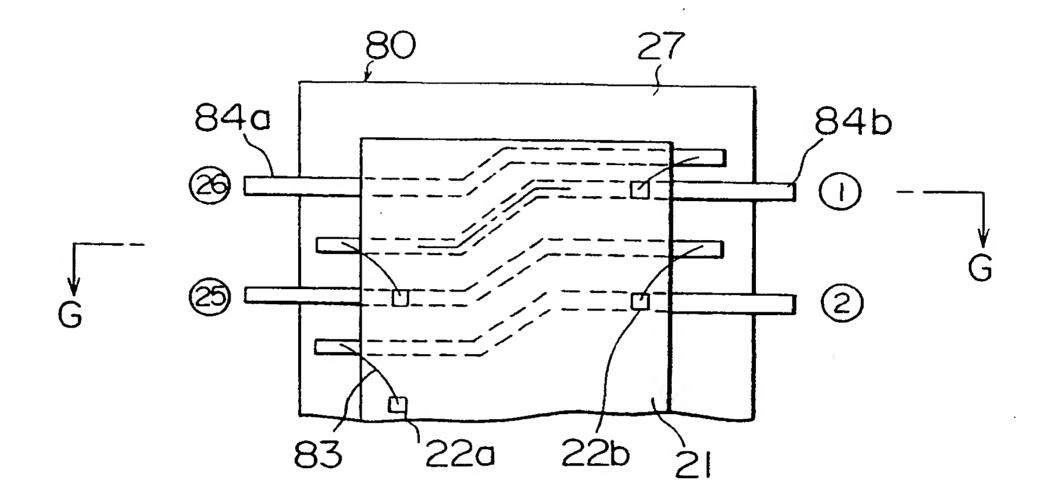


FIG .15



F1G.16

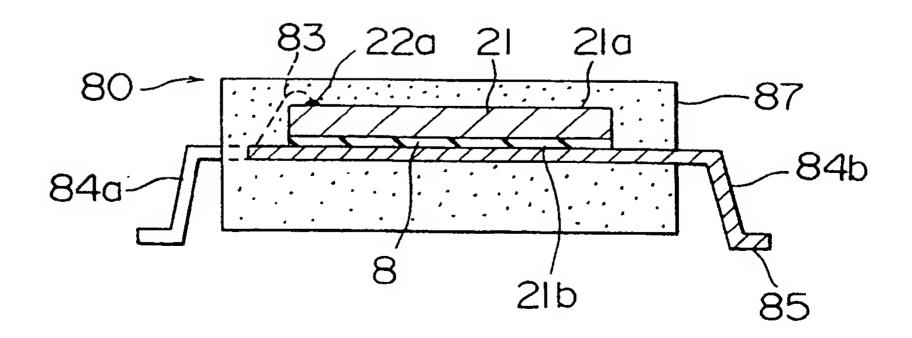


FIG.17

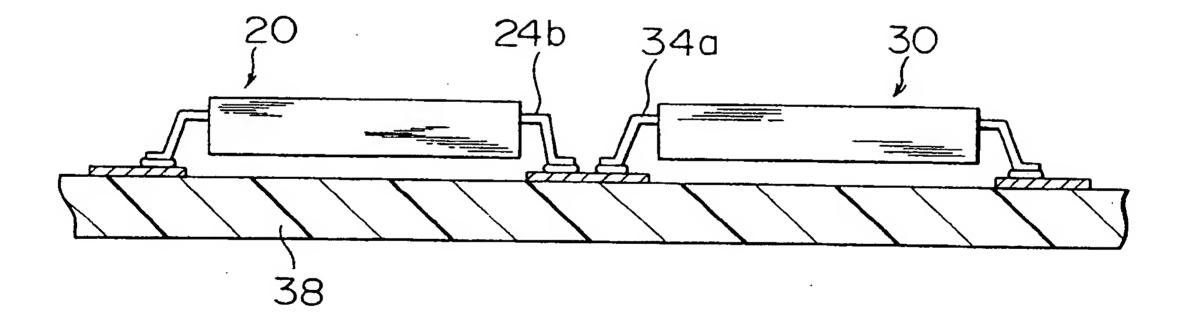


FIG.18 PRIOR ART

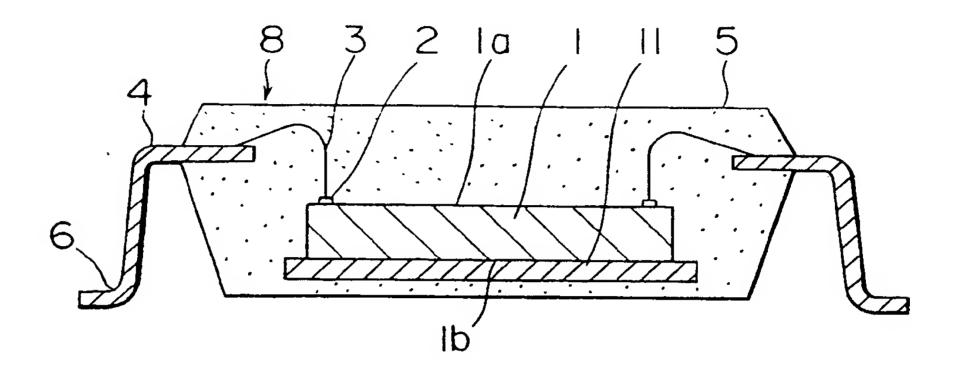
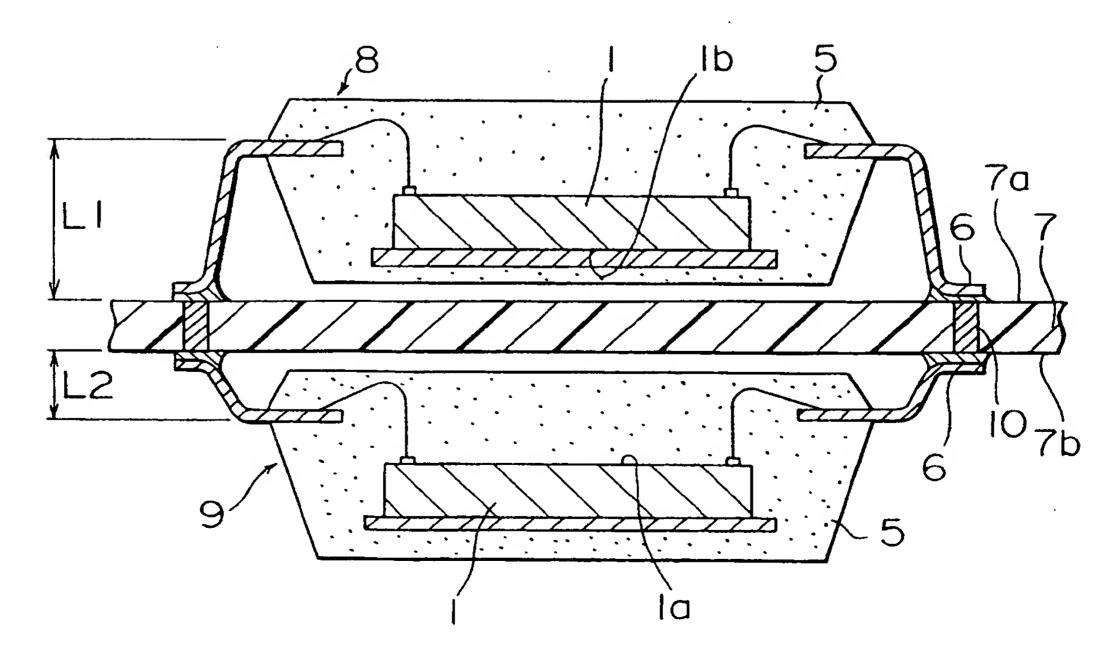


FIG.19 PRIOR ART



EP 0 538 003 A1



EUROPEAN SEARCH REPORT

Application Number

EP 92 30 9354

Category	Citation of document with i	ndication, where appropriate,	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X Y	DE-A-3 913 221 (MITSUBISHI DENKI K.K.) * figures *		1 1,2,4,8, 9,12,16, 17,20 3	H01L23/495 H05K1/18 H01L23/485 H01L25/10
Y A	EP-A-0 430 204 (KAB * figure 2 *	USHIKI KAISHA TOSHIBA)	1,2 5,6,13,	
Y	US-A-4 994 896 (SHU	NICHI UEMURA ET AL.) *	1,4,8,9, 12,16, 17,20	
A	GB-A-2 115 220 (HIT * abstract; figure		7,15	
A	PROCEEDINGS OF THE ELECTRONIC COMPONENTS CONFERENCE, Los Angeles, CA, 9th-11th May 1988, IEEE, New York, US, pages 552-557; W.C. Ward: "Volume production of unique plastic surface-mount modules for the IBM 80-ns 1-Mbit DRAM chip by area wire bond techniques." * figures *			TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L H05K
Р,Х	PATENT ABSTRACTS OF vol. 16, no. 45 (E-& JP-A-32 50 637 (November 1991 * abstract *	1162)5 February 1992	1	
	The present search report has l	peen drawn up for all claims Date of completion of the search		Pocani ner
•	Place of search THE HAGUE	01 FEBRUARY 1993		DE LAERE A.L.
X: par Y: par do: A: tec	CATEGORY OF CITED DOCUME rticularly relevant if taken alone rticularly relevant if combined with an nument of the same category chological background n-written disclosure	E : earlier patent after the filing other D : document cite L : document cite	d in the application d for other reasons	lished on, or

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